

# BEST AVAILABLE COPY

## PATENT ABSTRACTS OF JAPAN

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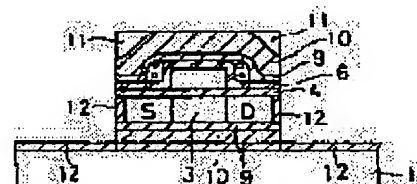
### (54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

#### (57)Abstract:

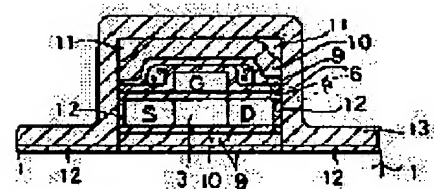
**PURPOSE:** To provide a semiconductor device having no leakage current in a P-N junction region in the device and a method for manufacturing the same to be formed on an SOI substrate.

**CONSTITUTION:** In a semiconductor device formed on an SOI substrate in which a single crystalline semiconductor layer 3 is formed on a semiconductor substrate 1 through an insulating film, all P-N junction regions of the device are protected by thermal oxide films 9, 12.

(a)



(b)



### LEGAL STATUS

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## CLAIMS

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### [Claim(s)]

[Claim 1] The semiconductor device characterized by coming to surround the PN-junction field established in said semiconductor device with the thermal oxidation film (9-12) in said semiconductor substrate (1) top in the semiconductor device which it comes to form in the SOI substrate with which it comes to form a single crystal half conductor layer (3) on a semiconductor substrate (1) through an insulator layer (2).

[Claim 2] Patterning of the SOI substrate with which the semiconductor device was formed in the SOI substrate with which it comes to form a single crystal half conductor layer (3) on a semiconductor substrate (1) through an insulator layer (2), and this semiconductor device was formed is carried out. Said single crystal half conductor layer (3) and insulator layer (2) of a semiconductor device formation field are remained in the shape of a mesa. After supporting the single crystal half conductor layer (3) and insulator layer (2) which remain in the shape of [ this ] a mesa with supporters (7), Remove said insulator layer (2) of said semiconductor device lower part, and a cavity (8) is formed. The manufacture approach of the semiconductor device characterized by having the process which embeds this cavity (8) and forms the thermal oxidation film (12) in the side attachment wall of said single-crystal-silicon layer (3) after forming the thermal oxidation film (9) in the wall of this cavity (8).

[Claim 3] Patterning of the SOI substrate with which it comes to form a single crystal half conductor layer (3) on a semiconductor substrate (1) through an insulator layer (2) is carried out. Said single crystal half conductor layer (3) and insulator layer (2) of a semiconductor device formation field are remained in the shape of a mesa. After supporting the single crystal half conductor layer (3) and insulator layer (2) which remain in the shape of [ this ] a mesa with supporters (7), Remove said insulator layer (2) of said semiconductor device formation field lower part, and a cavity (8) is formed. After forming the thermal oxidation film (9) in the wall of this cavity (8), this cavity (8) is embedded. The manufacture approach of the semiconductor device characterized by having the process which forms a semiconductor device in the single crystal half conductor layer (3) which remains in the shape of [ said ] a mesa, and forms the thermal oxidation film (12) in the side attachment wall of said single crystal half conductor layer (3).

[Claim 4] It is the manufacture approach of the semiconductor device according to claim 2 or 3 characterized by for said supporters' (7)'s ingredient being polycrystalline silicon or amorphous silicon, and the embedding ingredient of said cavity (8) being silicon oxide or polycrystalline silicon.

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## DETAILED DESCRIPTION

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### [Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a semiconductor device and its manufacture approach, the semiconductor device especially formed in a SOI substrate, and its manufacture approach.

[0002]

[Description of the Prior Art] With high integration of a semiconductor device, spacing between components becomes still narrower and the quality of separation between components influences the superiority or inferiority of an integrated circuit greatly. Moreover, formation of shallow junction is indispensable with high integration. Thin film SOI with which the thin single-crystal-silicon layer is formed through the insulator layer on the silicon substrate in order to fulfill these conditions (Silicon on Insulator) It is known that it is effective to use a substrate as a base material of a semiconductor device.

[0003] SIMOX which forms a diacid-ized silicone film on a silicon substrate using a CVD method, deposits a silicon layer on it, injects oxygen ion into melting, the approach of making it recrystallize and making it single-crystal-ize, or a silicon substrate, embeds this silicon layer at the approach of forming a SOI substrate, and forms an oxide film (Separation by Implanted Oxygen) There is law etc. There is also the approach of thin-film-izing one [ lamination and ] silicon substrate for the silicon substrate of two sheets mutually through an oxide film further again.

[0004] As an approach of forming a semiconductor device in these SOI substrates with which isolation was made, the approach of forming a semiconductor device and the same approach are used for the usual silicon substrate.

[0005]

[Problem(s) to be Solved by the Invention] By the way, leakage current is observed when for example, an MOS mold field-effect transistor (henceforth MOSFET) is formed in a thin film SOI substrate. Since the thickness of the single-crystal-silicon layer of a thin film SOI substrate is thinly formed in 1500A thickness extent, the PN-junction field of MOSFET is formed in contact with the insulator layer of a substrate. Consequently, it is thought that leakage current flows through the uncombined hand which exists in the interface of a PN-junction field and an insulator layer.

[0006] It has big effect on component actuation also by such minute leakage current, and it becomes impossible to fully demonstrate the advantage by using a thin film SOI substrate with high integration and low-power-izing.

[0007] In addition, also when making a SOI substrate into mesa mold structure and carrying out isolation, leakage current occurs in the interface of the protection insulator layer formed in a side attachment wall, and the PN-junction field formed in a side attachment wall.

[0008] The purpose of this invention is to cancel these faults, and has two purposes. The 1st purpose is formed on a thin film SOI substrate, and is to offer the semiconductor device which leakage current does not generate to a PN-junction field, and the 2nd purpose is to offer the manufacture approach.

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[0009]

[Means for Solving the Problem] The 1st purpose is attained among the two above-mentioned purposes by the semiconductor device by which the PN-junction field established in the aforementioned semiconductor device is surrounded with the thermal oxidation film (9-12) in the aforementioned semi-conductor substrate (1) top in the semiconductor device currently formed in the SOI substrate with which the single crystal half conductor layer (3) is formed through the insulator layer (2) on the semi-conductor substrate (1).

[0010] the 2nd purpose among the two above-mentioned purposes — the following — it is attained by any means. Patterning of the SOI substrate with which the 1st means formed the semiconductor device in the SOI substrate with which the single crystal half conductor layer (3) is formed through the insulator layer (2) on the semi-conductor substrate (1), and this semiconductor device was formed is carried out. The aforementioned single crystal half conductor layer (3) and aforementioned insulator layer (2) of a semiconductor device formation field are remained in the shape of a mesa. After supporting the single crystal half conductor layer (3) and insulator layer (2) which remain in the shape of [ this ] a mesa with supporters (7), Remove the aforementioned insulator layer (2) of the aforementioned semiconductor device lower part, and a cavity (8) is formed. After forming the thermal oxidation film (9) in the wall of this cavity (8), it is the manufacture approach of a semiconductor device of having the process which embeds this cavity (8) and forms the thermal oxidation film (12) in the side attachment wall of the aforementioned single-crystal-silicon layer (3).

[0011] The 2nd means carries out patterning of the SOI substrate with which the single crystal half conductor layer (3) is formed through the insulator layer (2) on the semi-conductor substrate (1). The aforementioned single crystal half conductor layer (3) and aforementioned insulator layer (2) of a semiconductor device formation field are remained in the shape of a mesa. After supporting the single crystal half conductor layer (3) and insulator layer (2) which remain in the shape of [ this ] a mesa with supporters (7), Remove the aforementioned insulator layer (2) of the aforementioned semiconductor device formation field lower part, and a cavity (8) is formed. After forming the thermal oxidation film (9) in the wall of this cavity (8), it is the manufacture approach of a semiconductor device of having the process which embeds this cavity (8), forms a semiconductor device in the single crystal half conductor layer (3) which remains in the shape of [ above ] a mesa, and forms the thermal oxidation film (12) in the side attachment wall of the aforementioned single crystal half conductor layer (3).

[0012] In addition, the aforementioned supporters' (7)'s ingredient is polycrystalline silicon or amorphous silicon, and, as for the embedding ingredient of the aforementioned cavity (8), it is desirable that they are silicon oxide or polycrystalline silicon.

[0013]

[Function] a CVD method when the insulator layer which constitutes a thin film SOI substrate is except the thermal oxidation film, and SIMOX — when formed using law etc., an uncombined hand exists in the interface of an insulator layer and a PN-junction field, and leakage current occurs to a PN-junction field through this uncombined hand. Then, the insulator layer which touches a PN-junction field can be altogether formed with the thermal oxidation film, and when making it an uncombined hand not exist in the interface of a PN-junction field and an insulator layer, the leakage current generated to a PN-junction field can be prevented.

[0014]

[Example] Hereafter, with reference to a drawing, the manufacture approach of the semiconductor device concerning two examples of this invention is explained.

[0015] it is shown in 1st example drawing 2 (a) — as — SIMOX — law, a lamination method, etc. are used and the SOI substrate with which the single-crystal-silicon layer 3 of 1500A thickness was formed through the diacid-ized silicon insulator layer 2 of 3000A thickness on the silicon substrate 1 is formed.

[0016] As shown in drawing 2 (b), it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 4 of about 100A thickness is formed, the reactive-ion-etching method which carries out laminating formation of the polycrystal silicone film of about 1000A thickness and the tungsten silicide film of about 500A thickness one by one, and subsequently makes

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carbon tetrafluoride reactant gas is used, patterning of the layered product of the aforementioned polycrystal silicone film and the tungsten silicide film is carried out, and the gate electrode 5 is formed.

[0017] As shown in drawing 3 (a), the gate electrode 5 is used as a mask and arsenic ion is driven in, and they are energy 50KeV and dose  $3 \times 10^{13} / \text{cm}^2$ . It has, and an ion implantation is carried out and Source S and Drain D are formed.

[0018] As shown in drawing 3 (b), the silicon nitride film 6 of 1000A thickness is formed in the whole surface using a plasma-CVD method, subsequently, a reactive-ion-etching method is used, the diacid-ized silicone film 2 and 4 are etched [ a silicon nitride film 6 ] for the single-crystal-silicon layer 3 using the mixed gas of carbon tetrafluoride and hydrogen using a carbon tetrachloride, respectively using the mixed gas of carbon tetrafluoride and hydrogen, and a component formation field is remained in the shape of a mesa.

[0019] As shown in drawing 4 (a), polycrystalline silicon is deposited on 2000A thickness using a heat CVD method, and supporters 7 are formed. As shown in drawing 4 (b), the supporters 7 who make reactive ion etching and consist of polycrystalline silicon currently formed in the both-ends side (space a vertical near side and a back side) of a mesa-like component formation field are removed, subsequently, the diacid-ized silicon insulator layer 2 is removed 1% using the fluoric acid liquid of concentration, and a cavity 8 is formed.

[0020] As shown in drawing 5 (a), the supporters 7 who consist of polycrystalline silicon using reactive ion etching are etched, and supporters 7 are remained only on the side attachment wall of a mesa-like component formation field.

[0021] As shown in drawing 5 (b), it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 9 of 100A thickness is formed in the front face of supporters 7 and a silicon substrate 1 at the inside list of a cavity 8, respectively.

[0022] As shown in drawing 6 (a), the diacid-ized silicon layer 10 is formed in 1500A thickness using a heat CVD method. Since a heat CVD method is isotropy, a cavity 8 is completely embedded with the diacid-ized silicon layer 10.

[0023] As shown in drawing 6 (b), liquid glass 11, such as OCD and SOG, is applied and flattening of the front face is carried out. As shown in drawing 1 (a), reactive ion etching is made, it remains in the shape of a mesa, a component formation field is oxidized thermally at the temperature of 850 degrees C, and the thermal oxidation film 12 is formed in the side attachment wall of the single-crystal-silicon layer 3.

[0024] As shown in drawing 1 (b), the diacid-ized silicone film 13 is formed using a heat CVD method. Hereafter, although not illustrated, an electrode and wiring are formed using the well-known approach.

[0025] The SOI substrate with which the single-crystal-silicon layer 3 is formed through the diacid-ized silicon insulator layer 2 at 2nd example drawing 7 (a) on the silicon substrate 1 is shown.

[0026] As shown in drawing 7 (b), a silicon nitride film 6 is formed on the single-crystal-silicon layer 3 at 1000A thickness using a plasma-CVD method. As shown in drawing 8 (a), a reactive-ion-etching method is used, the diacid-ized silicone film 2 is etched [ a silicon nitride film 6 ] for the single-crystal-silicon layer 3 using the mixed gas of carbon tetrafluoride and hydrogen using a carbon tetrachloride, respectively using the mixed gas of carbon tetrafluoride and hydrogen, and a component formation schedule field is remained with a width of face of 5 micrometers in the shape of a mesa.

[0027] As shown in drawing 8 (b), polycrystalline silicon is deposited on 2000A thickness using a heat CVD method, and supporters 7 are formed. As shown in drawing 9 (a), the supporters 7 who consist of polycrystalline silicon which makes reactive ion etching and is formed in the both-ends side (space a vertical near side and a back side) of a mesa-like component formation schedule field are removed, subsequently, the diacid-ized silicone film 2 is removed 1% using the fluoric acid liquid of concentration, and a cavity 8 is formed.

[0028] As shown in drawing 9 (b), supporters 7 are etched using a reactive-ion-etching method, and supporters 7 are remained on the side attachment wall of the single-crystal-silicon layer 3 and a silicon nitride film 6.

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[0029] As shown in drawing 10 (a), it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 9 is formed in the inside of a cavity 8, supporters' 7 front face, and the front face of a silicon substrate 1 at 100A thickness, respectively.

[0030] As shown in drawing 10 (b), the diacid-ized silicon layer 10 is formed in 1500A thickness using a heat CVD method. Since a heat CVD method is isotropy, the inside of a cavity 8 is completely embedded with the diacid-ized silicon layer 10.

[0031] As shown in drawing 11 (a), reactive ion etching is made and the diacid-ized silicon layer 10 and the thermal oxidation film 9 of a field except the inside of a cavity 8 are removed. As shown in drawing 11 (b), a silicon nitride film 6 is removed using a phosphoric acid, subsequently, it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 4 is formed in 150A thickness.

[0032] As shown in drawing 12 (a), the cascade screen of the polycrystal silicone film of 1000A thickness and the tungsten silicide film of 2000A thickness is formed, patterning of this cascade screen is carried out, the gate electrode 5 is formed, the gate electrode 5 is used as a mask, the ion implantation of the arsenic ion is carried out so that a damage may not be given to the thermal oxidation film 9 with impregnation energy 50KeV and a dose  $3 \times 10^{13}$ , and Source S and Drain D are formed.

[0033] As shown in drawing 12 (b), the diacid-ized silicon layer 14 is formed in 5000A thickness using a heat CVD method, subsequently, liquid glass 11, such as OCD and SOG, is applied and flattening of the front face is carried out.

[0034] As shown in drawing 13 (a), reactive ion etching is made and a component formation field is formed in the shape of a mesa. Subsequently, it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 12 of 100A thickness is formed in the side attachment wall of the single-crystal-silicon layer 3, and the front face of a silicon substrate 1. In addition, in this thermal oxidation process, the activation of an arsenic by which the ion implantation is previously carried out to the source drain field is made by coincidence.

[0035] As shown in drawing 13 (b), the diacid-ized silicon protective coat 13 is formed using a heat CVD method. Hereafter, although not illustrated, an electrode and wiring are formed using the well-known approach.

[0036]

[Effect of the Invention] In the semiconductor device applied to this invention as explained above, and its manufacture approach Since he is trying for an uncombined hand not to exist in the interface of a PN-junction field and the thermal oxidation film by protecting the PN-junction field of a semiconductor device with the thermal oxidation film altogether It is lost that leakage current occurs to a PN-junction field, the advantage by using a SOI substrate is demonstrated enough, a degree of integration is high and a semiconductor device with a good property is obtained.

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## TECHNICAL PROBLEM

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[Problem(s) to be Solved by the Invention] By the way, leakage current is observed when for example, an MOS mold field-effect transistor (henceforth MOSFET) is formed in a thin film SOI substrate. Since the thickness of the single-crystal-silicon layer of a thin film SOI substrate is thinly formed in 1500A thickness extent, the PN-junction field of MOSFET is formed in contact with the insulator layer of a substrate. Consequently, it is thought that leakage current flows through the uncombined hand which exists in the interface of a PN-junction field and an insulator layer.

[0006] It has big effect on component actuation also by such minute leakage current, and it becomes impossible to fully demonstrate the advantage by using a thin film SOI substrate with high integration and low-power-izing.

[0007] In addition, also when making a SOI substrate into mesa mold structure and carrying out isolation, leakage current occurs in the interface of the protection insulator layer formed in a side attachment wall, and the PN-junction field formed in a side attachment wall.

[0008] The purpose of this invention is to cancel these faults, and has two purposes. The 1st purpose is formed on a thin film SOI substrate, and is to offer the semiconductor device which leakage current does not generate to a PN-junction field, and the 2nd purpose is to offer the manufacture approach.

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MEANS

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[Means for Solving the Problem] The 1st purpose is attained among the two above-mentioned purposes by the semiconductor device by which the PN-junction field established in the aforementioned semiconductor device is surrounded with the thermal oxidation film (9-12) in the aforementioned semi-conductor substrate (1) top in the semiconductor device currently formed in the SOI substrate with which the single crystal half conductor layer (3) is formed through the insulator layer (2) on the semi-conductor substrate (1).

[0010] the 2nd purpose among the two above-mentioned purposes -- the following -- it is attained by any means. Patterning of the SOI substrate with which the 1st means formed the semiconductor device in the SOI substrate with which the single crystal half conductor layer (3) is formed through the insulator layer (2) on the semi-conductor substrate (1), and this semiconductor device was formed is carried out. The aforementioned single crystal half conductor layer (3) and aforementioned insulator layer (2) of a semiconductor device formation field are remained in the shape of a mesa. After supporting the single crystal half conductor layer (3) and insulator layer (2) which remain in the shape of [ this ] a mesa with supporters (7), Remove the aforementioned insulator layer (2) of the aforementioned semiconductor device lower part, and a cavity (8) is formed. After forming the thermal oxidation film (9) in the wall of this cavity (8), it is the manufacture approach of a semiconductor device of having the process which embeds this cavity (8) and forms the thermal oxidation film (12) in the side attachment wall of the aforementioned single-crystal-silicon layer (3).

[0011] The 2nd means carries out patterning of the SOI substrate with which the single crystal half conductor layer (3) is formed through the insulator layer (2) on the semi-conductor substrate (1). The aforementioned single crystal half conductor layer (3) and aforementioned insulator layer (2) of a semiconductor device formation field are remained in the shape of a mesa. After supporting the single crystal half conductor layer (3) and insulator layer (2) which remain in the shape of [ this ] a mesa with supporters (7), Remove the aforementioned insulator layer (2) of the aforementioned semiconductor device formation field lower part, and a cavity (8) is formed. After forming the thermal oxidation film (9) in the wall of this cavity (8), it is the manufacture approach of a semiconductor device of having the process which embeds this cavity (8), forms a semiconductor device in the single crystal half conductor layer (3) which remains in the shape of [ above ] a mesa, and forms the thermal oxidation film (12) in the side attachment wall of the aforementioned single crystal half conductor layer (3).

[0012] In addition, the aforementioned supporters' (7)'s ingredient is polycrystalline silicon or amorphous silicon, and, as for the embedding ingredient of the aforementioned cavity (8), it is desirable that they are silicon oxide or polycrystalline silicon.

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OPERATION

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[Function] a CVD method when the insulator layer which constitutes a thin film SOI substrate is except the thermal oxidation film, and SIMOX -- when formed using law etc., an uncombined hand exists in the interface of an insulator layer and a PN-junction field, and leakage current occurs to a PN-junction field through this uncombined hand. Then, the insulator layer which touches a PN-junction field can be altogether formed with the thermal oxidation film, and when making it an uncombined hand not exist in the interface of a PN-junction field and an insulator layer, the leakage current generated to a PN-junction field can be prevented.

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EXAMPLE

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[Example] Hereafter, with reference to a drawing, the manufacture approach of the semiconductor device concerning two examples of this invention is explained.

[0015] it is shown in 1st example drawing 2 (a) — as — SIMOX — law, a lamination method, etc. are used and the SOI substrate with which the single-crystal-silicon layer 3 of 1500A thickness was formed through the diacid-ized silicon insulator layer 2 of 3000A thickness on the silicon substrate 1 is formed.

[0016] As shown in drawing 2 (b), it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 4 of about 100A thickness is formed, the reactive-ion-etching method which carries out laminating formation of the polycrystal silicone film of about 1000A thickness and the tungsten silicide film of about 500A thickness one by one, and subsequently makes carbon tetrafluoride reactant gas is used, patterning of the layered product of the aforementioned polycrystal silicone film and the tungsten silicide film is carried out, and the gate electrode 5 is formed.

[0017] As shown in drawing 3 (a), the gate electrode 5 is used as a mask and arsenic ion is driven in, and they are energy 50KeV and dose  $3 \times 10^{13}$ —/cm<sup>2</sup>. It has, and an ion implantation is carried out and Source S and Drain D are formed.

[0018] As shown in drawing 3 (b), the silicon nitride film 6 of 1000A thickness is formed in the whole surface using a plasma-CVD method, subsequently, a reactive-ion-etching method is used, the diacid-ized silicone film 2 and 4 are etched [ a silicon nitride film 6 ] for the single-crystal-silicon layer 3 using the mixed gas of carbon tetrafluoride and hydrogen using a carbon tetrachloride, respectively using the mixed gas of carbon tetrafluoride and hydrogen, and a component formation field is remained in the shape of a mesa.

[0019] As shown in drawing 4 (a), polycrystalline silicon is deposited on 2000A thickness using a heat CVD method, and supporters 7 are formed. As shown in drawing 4 (b), the supporters 7 who make reactive ion etching and consist of polycrystalline silicon currently formed in the both-ends side (space a vertical near side and a back side) of a mesa-like component formation field are removed, subsequently, the diacid-ized silicon insulator layer 2 is removed 1% using the fluoric acid liquid of concentration, and a cavity 8 is formed.

[0020] As shown in drawing 5 (a), the supporters 7 who consist of polycrystalline silicon using reactive ion etching are etched, and supporters 7 are remained only on the side attachment wall of a mesa-like component formation field.

[0021] As shown in drawing 5 (b), it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 9 of 100A thickness is formed in the front face of supporters 7 and a silicon substrate 1 at the inside list of a cavity 8, respectively.

[0022] As shown in drawing 6 (a), the diacid-ized silicon layer 10 is formed in 1500A thickness using a heat CVD method. Since a heat CVD method is isotropy, a cavity 8 is completely embedded with the diacid-ized silicon layer 10.

[0023] As shown in drawing 6 (b), liquid glass 11, such as OCD and SOG, is applied and flattening of the front face is carried out. As shown in drawing 1 (a), reactive ion etching is made, it remains in the shape of a mesa, a component formation field is oxidized thermally at the temperature of 850 degrees C, and the thermal oxidation film 12 is formed in the side

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attachment wall of the single-crystal-silicon layer 3.

[0024] As shown in drawing 1 (b), the diacid-ized silicone film 13 is formed using a heat CVD method. Hereafter, although not illustrated, an electrode and wiring are formed using the well-known approach.

[0025] The SOI substrate with which the single-crystal-silicon layer 3 is formed through the diacid-ized silicon insulator layer 2 at 2nd example drawing 7 (a) on the silicon substrate 1 is shown.

[0026] As shown in drawing 7 (b), a silicon nitride film 6 is formed on the single-crystal-silicon layer 3 at 1000A thickness using a plasma-CVD method. As shown in drawing 8 (a), a reactive-ion-etching method is used, the diacid-ized silicone film 2 is etched [ a silicon nitride film 6 ] for the single-crystal-silicon layer 3 using the mixed gas of carbon tetrafluoride and hydrogen using a carbon tetrachloride, respectively using the mixed gas of carbon tetrafluoride and hydrogen, and a component formation schedule field is remained with a width of face of 5 micrometers in the shape of a mesa.

[0027] As shown in drawing 8 (b), polycrystalline silicon is deposited on 2000A thickness using a heat CVD method, and supporters 7 are formed. As shown in drawing 9 (a), the supporters 7 who consist of polycrystalline silicon which makes reactive ion etching and is formed in the both-ends side (space a vertical near side and a back side) of a mesa-like component formation schedule field are removed, subsequently, the diacid-ized silicone film 2 is removed 1% using the fluoric acid liquid of concentration, and a cavity 8 is formed.

[0028] As shown in drawing 9 (b), supporters 7 are etched using a reactive-ion-etching method, and supporters 7 are remained on the side attachment wall of the single-crystal-silicon layer 3 and a silicon nitride film 6.

[0029] As shown in drawing 10 (a), it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 9 is formed in the inside of a cavity 8, supporters' 7 front face, and the front face of a silicon substrate 1 at 100A thickness, respectively.

[0030] As shown in drawing 10 (b), the diacid-ized silicon layer 10 is formed in 1500A thickness using a heat CVD method. Since a heat CVD method is isotropy, the inside of a cavity 8 is completely embedded with the diacid-ized silicon layer 10.

[0031] As shown in drawing 11 (a), reactive ion etching is made and the diacid-ized silicon layer 10 and the thermal oxidation film 9 of a field except the inside of a cavity 8 are removed. As shown in drawing 11 (b), a silicon nitride film 6 is removed using a phosphoric acid, subsequently, it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 4 is formed in 150A thickness.

[0032] As shown in drawing 12 (a), the cascade screen of the polycrystal silicone film of 1000A thickness and the tungsten silicide film of 2000A thickness is formed, patterning of this cascade screen is carried out, the gate electrode 5 is formed, the gate electrode 5 is used as a mask, the ion implantation of the arsenic ion is carried out so that a damage may not be given to the thermal oxidation film 9 with impregnation energy 50KeV and a dose  $3 \times 10^{13}$ , and Source S and Drain D are formed.

[0033] As shown in drawing 12 (b), the diacid-ized silicon layer 14 is formed in 5000A thickness using a heat CVD method, subsequently, liquid glass 11, such as OCD and SOG, is applied and flattening of the front face is carried out.

[0034] As shown in drawing 13 (a), reactive ion etching is made and a component formation field is formed in the shape of a mesa. Subsequently, it oxidizes thermally at the temperature of 850 degrees C, and the thermal oxidation film 12 of 100A thickness is formed in the side attachment wall of the single-crystal-silicon layer 3, and the front face of a silicon substrate 1. In addition, in this thermal oxidation process, the activation of an arsenic by which the ion implantation is previously carried out to the source drain field is made by coincidence.

[0035] As shown in drawing 13 (b), the diacid-ized silicon protective coat 13 is formed using a heat CVD method. Hereafter, although not illustrated, an electrode and wiring are formed using the well-known approach.

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## DESCRIPTION OF DRAWINGS

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### [Brief Description of the Drawings]

[Drawing 1] It is the production process Fig. (the 6) of the semiconductor device concerning the 1st example of this invention.

[Drawing 2] It is the production process Fig. (the 1) of the semiconductor device concerning the 1st example of this invention.

[Drawing 3] It is the production process Fig. (the 2) of the semiconductor device concerning the 1st example of this invention.

[Drawing 4] It is the production process Fig. (the 3) of the semiconductor device concerning the 1st example of this invention.

[Drawing 5] It is the production process Fig. (the 4) of the semiconductor device concerning the 1st example of this invention.

[Drawing 6] It is the production process Fig. (the 5) of the semiconductor device concerning the 1st example of this invention.

[Drawing 7] It is the production process Fig. (the 1) of the semiconductor device concerning the 2nd example of this invention.

[Drawing 8] It is the production process Fig. (the 2) of the semiconductor device concerning the 2nd example of this invention.

[Drawing 9] It is the production process Fig. (the 3) of the semiconductor device concerning the 2nd example of this invention.

[Drawing 10] It is the production process Fig. (the 4) of the semiconductor device concerning the 2nd example of this invention.

[Drawing 11] It is the production process Fig. (the 5) of the semiconductor device concerning the 2nd example of this invention.

[Drawing 12] It is the production process Fig. (the 6) of the semiconductor device concerning the 2nd example of this invention.

[Drawing 13] It is the production process Fig. (the 7) of the semiconductor device concerning the 2nd example of this invention.

### [Description of Notations]

1 Semi-conductor Substrate (Silicon Substrate)

2 Insulator Layer (Diacid-ized Silicone Film)

3 Single Crystal Half Conductor Layer (Single-Crystal-Silicon Layer)

4 Thermal Oxidation Film

5 Gate

6 Silicon Nitride Film

7 Supporters (Polycrystalline Silicon Layer)

8 Cavity

9 Thermal Oxidation Film

10 Diacid-ized Silicon Layer

11 Liquid Glass Layer

12 Thermal Oxidation Film

13-14 Diacid-ized silicone film

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S Source

D Drain

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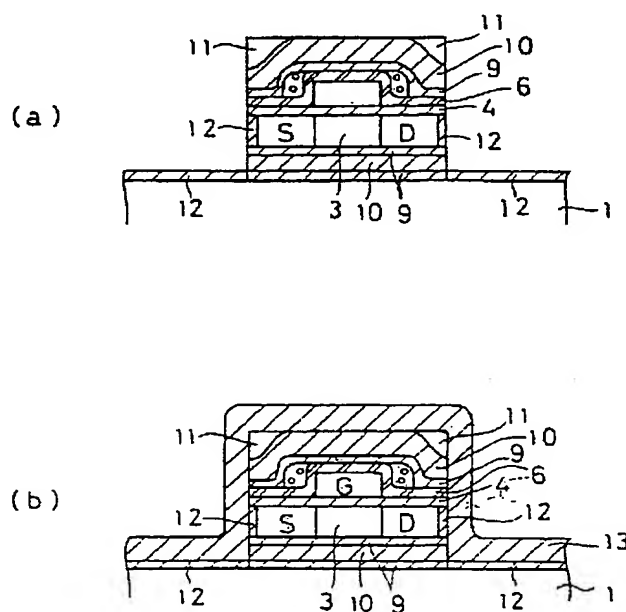
(54)【発明の名称】 半導体装置及びその製造方法

(57)【要約】

【目的】 半導体装置及びその製造方法、特に、S O I 基板に形成される半導体装置及びその製造方法に関し、P N接合領域にリーク電流が発生することのない半導体装置を提供することを目的とする。

【構成】 半導体基板 1 上に絶縁膜 2 を介して単結晶半導体層 3 が形成されている S O I 基板に形成される半導体装置において、半導体装置のすべての P N接合領域を熱酸化膜 9・12をもって保護するように構成する。

第 1 実施例工程図 (その 6)



## 【特許請求の範囲】

【請求項1】 半導体基板（1）上に絶縁膜（2）を介して単結晶半導体層（3）が形成されてなるSOI基板に形成されてなる半導体装置において、前記半導体装置に設けられたPN接合領域が前記半導体基板（1）上において熱酸化膜（9・12）をもって包囲されてなることを特徴とする半導体装置。

【請求項2】 半導体基板（1）上に絶縁膜（2）を介して単結晶半導体層（3）が形成されてなるSOI基板に半導体素子を形成し、  
該半導体素子の形成されたSOI基板をパターンニングして、半導体素子形成領域の前記単結晶半導体層（3）と絶縁膜（2）とをメサ状に残留し、

該メサ状に残留する単結晶半導体層（3）と絶縁膜（2）とを支持層（7）をもって支持した後、前記半導体素子下部の前記絶縁膜（2）を除去して空洞（8）を形成し、

該空洞（8）の内壁に熱酸化膜（9）を形成した後、該空洞（8）を埋め込み、

前記単結晶シリコン層（3）の側壁に熱酸化膜（12）を形成する工程を有することを特徴とする半導体装置の製造方法。

【請求項3】 半導体基板（1）上に絶縁膜（2）を介して単結晶半導体層（3）が形成されてなるSOI基板をパターンニングして、半導体素子形成領域の前記単結晶半導体層（3）と絶縁膜（2）とをメサ状に残留し、  
該メサ状に残留する単結晶半導体層（3）と絶縁膜（2）とを支持層（7）をもって支持した後、前記半導体素子形成領域下部の前記絶縁膜（2）を除去して空洞（8）を形成し、

該空洞（8）の内壁に熱酸化膜（9）を形成した後、該空洞（8）を埋め込み、

前記メサ状に残留する単結晶半導体層（3）に半導体素子を形成し、  
前記単結晶半導体層（3）の側壁に熱酸化膜（12）を形成する工程を有することを特徴とする半導体装置の製造方法。

【請求項4】 前記支持層（7）の材料は多結晶シリコンまたは非晶質シリコンであり、前記空洞（8）の埋め込み材料は酸化シリコンまたは多結晶シリコンであることを特徴とする請求項2または3記載の半導体装置の製造方法。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】本発明は、半導体装置及びその製造方法、特に、SOI基板に形成される半導体装置及びその製造方法に関する。

## 【0002】

【従来の技術】半導体装置の高集積化にともなって素子相互間の間隔は益々狭くなり、素子間の分離の良否が集

積回路の優劣を大きく左右するようになっている。また、高集積化にともなって浅い接合の形成が不可欠になっている。これらの条件を満たすには、シリコン基板上に絶縁膜を介して薄い単結晶シリコン層が形成されている薄膜SOI（Silicon on Insulator）基板を半導体装置の母材として使用することが有効であることが知られている。

【0003】SOI基板を形成する方法には、シリコン基板上にCVD法を使用して二酸化シリコン膜を形成し、その上にシリコン層を堆積し、このシリコン層を溶融・再結晶化させて単結晶化させる方法、または、シリコン基板に酸素イオンを注入して埋め込み酸化膜を形成するSIMOX（Separation by Implanted Oxygen）法等がある。さらにまた、2枚のシリコン基板を酸化膜を介して相互に張り合わせ、一方のシリコン基板を薄膜化する方法もある。

【0004】素子分離のなされたこれらのSOI基板に半導体素子を形成する方法としては、通常のシリコン基板に半導体素子を形成する方法と同じ方法が使用されている。

## 【0005】

【発明が解決しようとする課題】ところで、薄膜SOI基板に、例えば、MOS型電界効果トランジスタ（以下、MOSFETと云う。）を形成した場合にリーク電流が観察される。薄膜SOI基板の単結晶シリコン層の厚さは1500Å厚程度に薄く形成されているので、MOSFETのPN接合領域は下地の絶縁膜に接して形成される。その結果、PN接合領域と絶縁膜との界面に存在する未結合手を介してリーク電流が流れるものと思われる。

【0006】高集積化、低消費電力化にともない、このような微小なリーク電流でも素子動作に大きな影響を与え、薄膜SOI基板を使用することによる長所を十分に発揮することができなくなる。

【0007】なお、SOI基板をメサ型構造にして素子分離をする場合にも、側壁に形成される保護絶縁膜と側壁に形成されるPN接合領域との界面にリーク電流が発生する。

【0008】本発明の目的は、これらの欠点を解消することであり、二つの目的を有する。第1の目的は、薄膜SOI基板上に形成され、PN接合領域にリーク電流が発生することのない半導体装置を提供することであり、第2の目的は、その製造方法を提供することにある。

## 【0009】

【課題を解決するための手段】上記二つの目的のうち、第1の目的は、半導体基板（1）上に絶縁膜（2）を介して単結晶半導体層（3）が形成されているSOI基板に形成されている半導体装置において、前記の半導体装置に設けられたPN接合領域が前記の半導体基板（1）上において熱酸化膜（9・12）をもって包囲されている



半導体装置によって達成される。

【0010】上記二つの目的のうち、第2の目的は、下記いずれの手段によっても達成される。第1の手段は、半導体基板(1)上に絶縁膜(2)を介して単結晶半導体層(3)が形成されているSOI基板に半導体素子を形成し、この半導体素子の形成されたSOI基板をパターンニングして、半導体素子形成領域の前記の単結晶半導体層(3)と絶縁膜(2)とをメサ状に残留し、このメサ状に残留する単結晶半導体層(3)と絶縁膜(2)とを支持層(7)をもって支持した後、前記の半導体素子下部の前記の絶縁膜(2)を除去して空洞(8)を形成し、この空洞(8)の内壁に熱酸化膜(9)を形成した後、この空洞(8)を埋め込み、前記の単結晶シリコン層(3)の側壁に熱酸化膜(12)を形成する工程を有する半導体装置の製造方法である。

【0011】第2の手段は、半導体基板(1)上に絶縁膜(2)を介して単結晶半導体層(3)が形成されているSOI基板をパターンニングして、半導体素子形成領域の前記の単結晶半導体層(3)と絶縁膜(2)とをメサ状に残留し、このメサ状に残留する単結晶半導体層

(3)と絶縁膜(2)とを支持層(7)をもって支持した後、前記の半導体素子形成領域下部の前記の絶縁膜(2)を除去して空洞(8)を形成し、この空洞(8)の内壁に熱酸化膜(9)を形成した後、この空洞(8)を埋め込み、前記のメサ状に残留する単結晶半導体層(3)に半導体素子を形成し、前記の単結晶半導体層(3)の側壁に熱酸化膜(12)を形成する工程を有する半導体装置の製造方法である。

【0012】なお、前記の支持層(7)の材料は多結晶シリコンまたは非晶質シリコンであり、前記の空洞(8)の埋め込み材料は酸化シリコンまたは多結晶シリコンであることが望ましい。

【0013】

【作用】薄膜SOI基板を構成する絶縁膜が熱酸化膜以外の場合、例えばCVD法、SIMOX法等を使用して形成される場合には、絶縁膜とPN接合領域との界面に未結合手が存在し、この未結合手を介してPN接合領域にリーク電流が発生する。そこで、PN接合領域に接する絶縁膜をすべて熱酸化膜をもって形成し、PN接合領域と絶縁膜との界面に未結合手が存在しないようにすることによってPN接合領域に発生するリーク電流を防ぐことができる。

【0014】

【実施例】以下、図面を参照して、本発明の二つの実施例に係る半導体装置の製造方法について説明する。

【0015】第1例

図2(a)に示すように、SIMOX法、張り合わせ法等を使用して、シリコン基板1上に3000Å厚の二酸化シリコン絶縁膜2を介して1500Å厚の単結晶シリコン層3が形成されたSOI基板を形成する。

【0016】図2(b)に示すように、850℃の温度で熱酸化して約100Å厚の熱酸化膜4を形成し、次いで、約1000Å厚の多結晶シリコン膜と約500Å厚のタングステンシリサイド膜とを順次積層形成し、四フッ化炭素を反応ガスとする反応性イオンエッチング法を使用して、前記の多結晶シリコン膜とタングステンシリサイド膜との積層体をパターンニングしてゲート電極5を形成する。

【0017】図3(a)に示すように、ゲート電極5をマスクにしてヒ素イオンを打ち込みエネルギー50KeV、ドーズ量 $3 \times 10^{13} / \text{cm}^2$ をもってイオン注入し、ソースSとドレインDとを形成する。

【0018】図3(b)に示すように、プラズマCVD法を使用して全面に1000Å厚の窒化シリコン膜6を形成し、次いで、反応性イオンエッチング法を使用し、四フッ化炭素と水素との混合ガスを使用して窒化シリコン膜6を、四塩化炭素を使用して単結晶シリコン層3を、四フッ化炭素と水素との混合ガスを使用して二酸化シリコン膜2・4をそれぞれエッチングして素子形成領域をメサ状に残留する。

【0019】図4(a)に示すように、熱CVD法を使用して多結晶シリコンを2000Å厚に堆積して支持層7を形成する。図4(b)に示すように、反応性イオンエッチングをなして、メサ状の素子形成領域の両端面(紙面に垂直方向の手前側と奥側)に形成されている多結晶シリコンよりなる支持層7を除去し、次いで、1%濃度のフッ酸液を使用して二酸化シリコン絶縁膜2を除去して空洞8を形成する。

【0020】図5(a)に示すように、反応性イオンエッチングを使用して多結晶シリコンよりなる支持層7をエッチングし、メサ状の素子形成領域の側壁のみに支持層7を残留する。

【0021】図5(b)に示すように、850℃の温度で熱酸化して100Å厚の熱酸化膜9を空洞8の内面並びに支持層7及びシリコン基板1の表面にそれぞれ形成する。

【0022】図6(a)に示すように、熱CVD法を使用して二酸化シリコン層10を1500Å厚に形成する。熱CVD法は等方性であるので、空洞8は二酸化シリコン層10をもって完全に埋め込まれる。

【0023】図6(b)に示すように、OCD、SOG等の液体ガラス11を塗布して表面を平坦化する。図1

(a)に示すように、反応性イオンエッチングをなし、素子形成領域をメサ状に残留し、850℃の温度で熱酸化して単結晶シリコン層3の側壁に熱酸化膜12を形成する。

【0024】図1(b)に示すように、熱CVD法を使用して二酸化シリコン膜13を形成する。以下、図示しないが、周知の方法を使用して電極・配線を形成する。

【0025】第2例

図7(a)に、シリコン基板1上に二酸化シリコン絶縁膜2を介して単結晶シリコン層3が形成されているSOI基板を示す。

【0026】図7(b)に示すように、プラズマCVD法を使用して単結晶シリコン層3上に窒化シリコン膜6を1000Å厚に形成する。図8(a)に示すように、反応性イオンエッチング法を使用し、四フッ化炭素と水素との混合ガスを使用して窒化シリコン膜6を、四塩化炭素を使用して単結晶シリコン層3を、四フッ化炭素と水素との混合ガスを使用して二酸化シリコン膜2をそれぞれエッチングして、素子形成予定領域を例えば幅5μmのメサ状に残留する。

【0027】図8(b)に示すように、熱CVD法を使用して多結晶シリコンを2000Å厚に堆積し、支持層7を形成する。図9(a)に示すように、反応性イオンエッチングをなしてメサ状の素子形成予定領域の両端面(紙面に垂直方向の手前側と奥側)に形成されている多結晶シリコンよりなる支持層7を除去し、次いで、1%濃度のフッ酸液を使用して二酸化シリコン膜2を除去して空洞8を形成する。

【0028】図9(b)に示すように、反応性イオンエッチング法を使用して支持層7をエッチングし、単結晶シリコン層3と窒化シリコン膜6との側壁に支持層7を残留する。

【0029】図10(a)に示すように、850℃の温度で熱酸化し、空洞8の内面と支持層7の表面とシリコン基板1の表面とにそれぞれ熱酸化膜9を100Å厚に形成する。

【0030】図10(b)に示すように、熱CVD法を使用して二酸化シリコン層10を1500Å厚に形成する。熱CVD法は等方性であるので、空洞8内は完全に二酸化シリコン層10をもって埋め込まれる。

【0031】図11(a)に示すように、反応性イオンエッチングをなして空洞8内を除く領域の二酸化シリコン層10と熱酸化膜9とを除去する。図11(b)に示すように、リン酸を使用して窒化シリコン膜6を除去し、次いで、850℃の温度で熱酸化して熱酸化膜4を150Å厚に形成する。

【0032】図12(a)に示すように、1000Å厚の多結晶シリコン膜と2000Å厚のタンゲステンシリサイド膜との積層膜を形成し、この積層膜をパターニングしてゲート電極5を形成し、ゲート電極5をマスクにしてヒ素イオンを注入エネルギー50KeV、ドーズ量3×10<sup>13</sup>をもって熱酸化膜9にダメージを与えないようにイオン注入してソースSとドレインDとを形成する。

【0033】図12(b)に示すように、熱CVD法を使用して二酸化シリコン層14を5000Å厚に形成し、次いで、OCD、SOG等の液体ガラス11を塗布して表面を平坦化する。

【0034】図13(a)に示すように、反応性イオンエ

ッチングをなして素子形成領域をメサ状に形成する。次いで、850℃の温度で熱酸化して100Å厚の熱酸化膜12を単結晶シリコン層3の側壁とシリコン基板1の表面とに形成する。なお、この熱酸化工程において、先にソース・ドレイン領域にイオン注入されているヒ素の活性化が同時になされる。

【0035】図13(b)に示すように、熱CVD法を使用して二酸化シリコン保護膜13を形成する。以下、図示しないが、周知の方法を使用して電極・配線を形成する。

【0036】

【発明の効果】以上説明したとおり、本発明に係る半導体装置及びその製造方法においては、半導体装置のPN接合領域をすべて熱酸化膜をもって保護することによってPN接合領域と熱酸化膜との界面に未結合手が存在しないようにしているので、PN接合領域にリーク電流が発生することがなくなり、SOI基板を使用することによる長所が十分発揮され、集積度が高く、特性の良好な半導体装置が得られる。

【図面の簡単な説明】

【図1】本発明の第1実施例に係る半導体装置の製造工程図(その6)である。

【図2】本発明の第1実施例に係る半導体装置の製造工程図(その1)である。

【図3】本発明の第1実施例に係る半導体装置の製造工程図(その2)である。

【図4】本発明の第1実施例に係る半導体装置の製造工程図(その3)である。

【図5】本発明の第1実施例に係る半導体装置の製造工程図(その4)である。

【図6】本発明の第1実施例に係る半導体装置の製造工程図(その5)である。

【図7】本発明の第2実施例に係る半導体装置の製造工程図(その1)である。

【図8】本発明の第2実施例に係る半導体装置の製造工程図(その2)である。

【図9】本発明の第2実施例に係る半導体装置の製造工程図(その3)である。

【図10】本発明の第2実施例に係る半導体装置の製造工程図(その4)である。

【図11】本発明の第2実施例に係る半導体装置の製造工程図(その5)である。

【図12】本発明の第2実施例に係る半導体装置の製造工程図(その6)である。

【図13】本発明の第2実施例に係る半導体装置の製造工程図(その7)である。

【符号の説明】

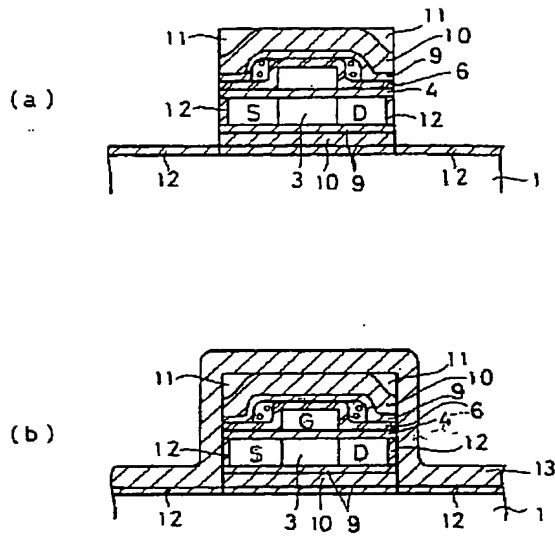
- 1 半導体基板(シリコン基板)
- 2 絶縁膜(二酸化シリコン膜)
- 3 単結晶半導体層(単結晶シリコン層)

- 4 熱酸化膜
- 5 ゲート
- 6 窒化シリコン膜
- 7 支持層 (多結晶シリコン層)
- 8 空洞
- 9 熱酸化膜

- 10 二酸化シリコン層
- 11 液体ガラス層
- 12 熱酸化膜
- 13・14 二酸化シリコン膜
- S ソース
- D ドレイン

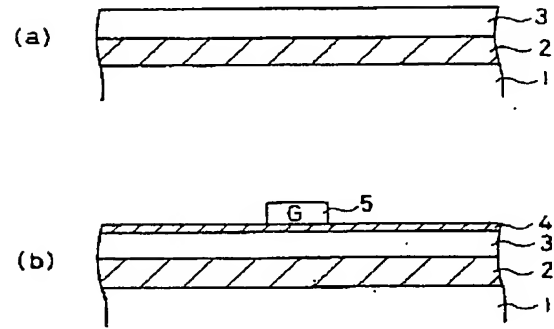
【図 1】

第 1 実施例工程図 (その 6)



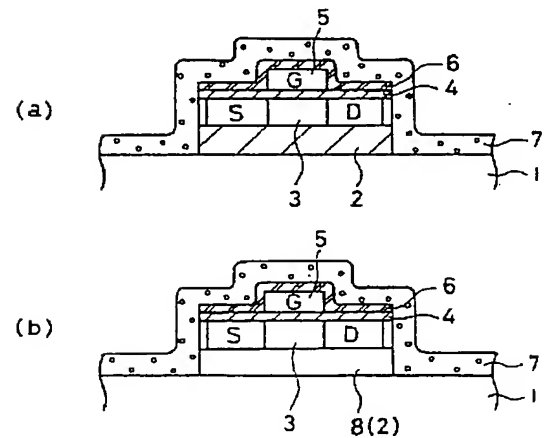
【図 2】

第 1 実施例工程図 (その 1)



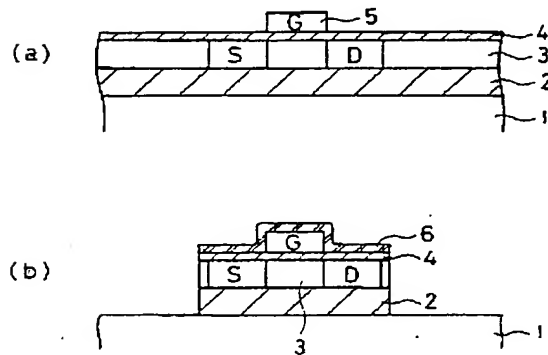
【図 4】

第 1 実施例工程図 (その 3)



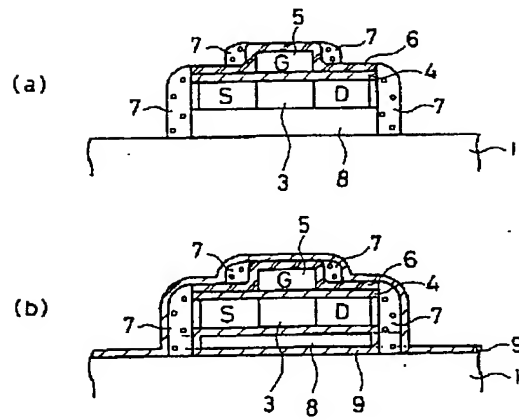
【図 3】

第 1 実施例工程図 (その 2)



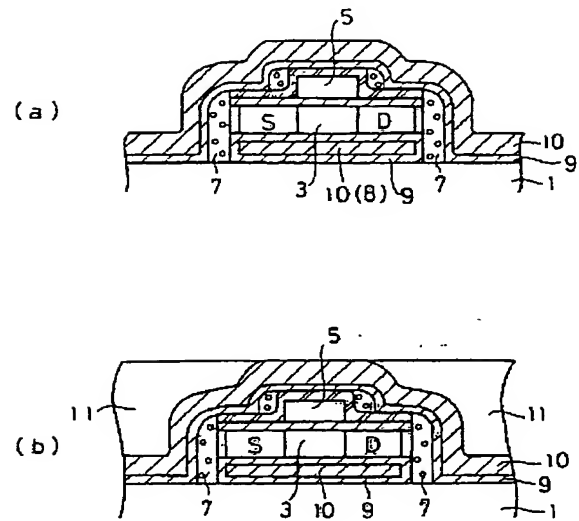
【図5】

第1実施例工程図（その4）



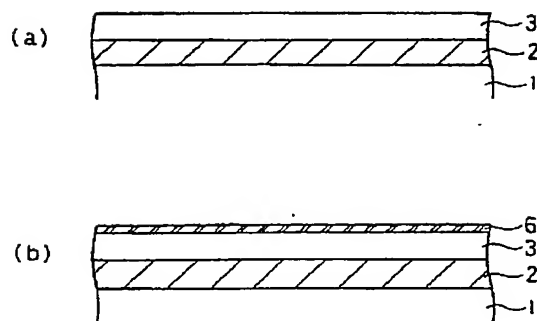
【図6】

第1実施例工程図（その5）



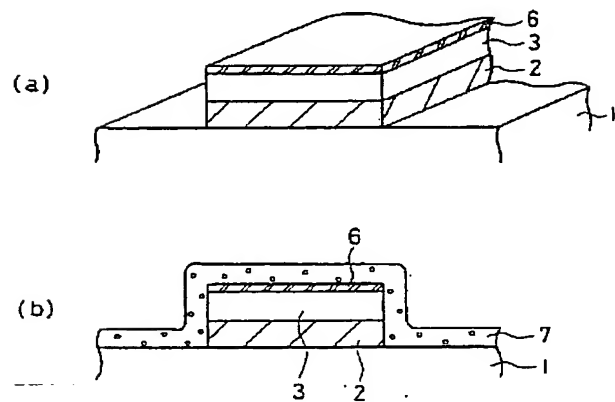
【図7】

第2実施例工程図（その1）



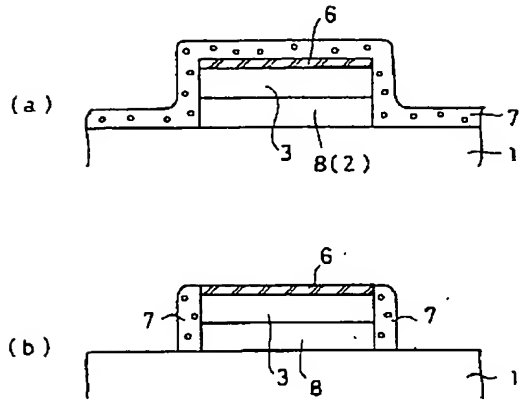
【図8】

第2実施例工程図（その2）



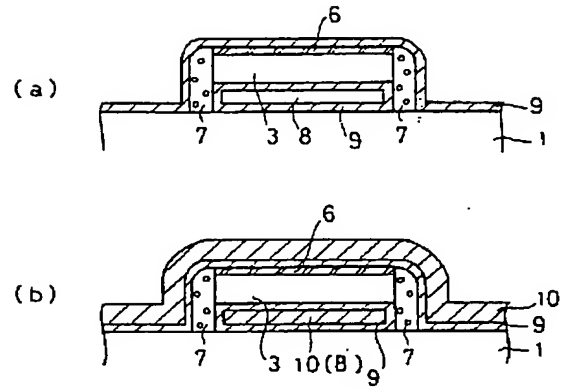
【図 9】

第 2 実施例工程図 (その 3)



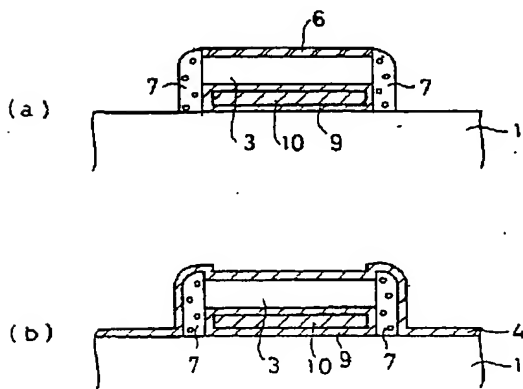
【図 10】

第 2 実施例工程図 (その 4)



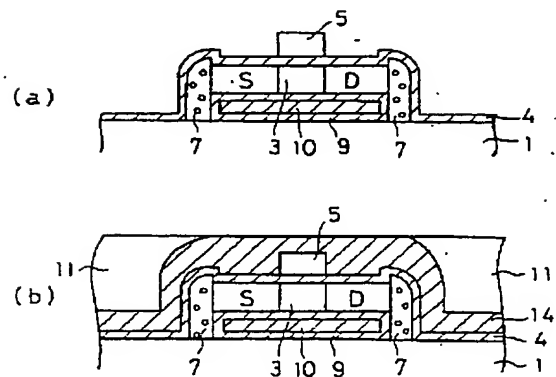
【図 11】

第 2 実施例工程図 (その 5)



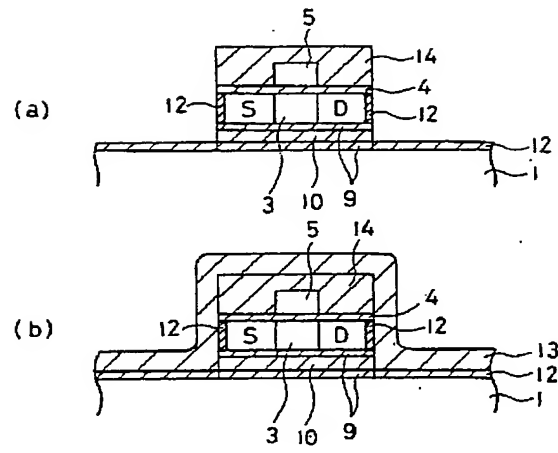
【図 12】

第 2 実施例工程図 (その 6)



【図13】

## 第2実施例工程図（その7）



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